layer can be changed to the opposite type to form a VJFET. As yet another example, double-sided epitaxial growth or double-sided ion implantation onto both sides of a bulk wafer of an appropriate thickness in the range of 100um to 400um and a doping density in the range of $10^{13}cm^{-3}$ to $10^{15}cm^{-3}$ can be used to implement the invention. As a further example, the vertical channel length, while described as 2.1um for up to 14kV VJFETs, can be smaller in designing lower voltage VJFETs as described in a paper published by J. H. Zhao et al. entitled *demonstration of a high performance 4H-SiC vertical junction field effect transistor without epitaxial regrowth* by IEE Electronics Letters, Vol.39, No.3, Feb. 6, 2003, pp.321-323, cited here as reference, which reports an experimental normally-on VJFET blocking 392V achieving a very low R_{sp} of 1.4 $m\Omega cm^2$ using a vertical channel length of 1.57um and a blocking layer of only 1.33um. As yet one more example, although SiC semiconductor is used as example of illustration, other semiconductors can be equally used to form the VJFET of the invention such as GaN, AlGaN, InGaN, diamond, AlGaAsP, Si, ZnO, MgZnO and the combinations thereof.

In the drawings and specifications described above, typical preferred embodiments have been disclosed of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and are not for purpose of limitation for the scope of the invention.

What is claimed is:

1. A semiconductor vertical junction field-effect power transistor formed by a semiconductor structure having top and bottom surfaces and including a plurality of

semiconductor layers with predetermined doping concentrations and thicknesses and comprising

(a) At least a bottom layer as drain layer of said transistor, a middle layer as blocking and channel layer of said transistor, a top layer as source layer of said transistor;

(b) a plurality of laterally spaced U-shaped trenches with highly vertical side walls defining a plurality of laterally spaced mesas in said semiconductor structure;

(c) said highly vertical side walls making an angle of β with respect to the said top surface of said semiconductor structure;

(d) said mesas surrounded on the four sides perpendicular to said top surface by U-shaped semiconductor regions; said U-shaped semiconductor regions having conductivity type opposite to the conductivity type of said mesas, forming U-shaped pn junctions; ;

(e) said U-shaped pn junctions having selectively and heavily doped regions formed on the bottom of said U-shaped pn junctions for the formation of gate ohmic contacts; said selectively and heavily doped regions having same conductivity type as said U-shaped semiconductor regions;

(f) said U-shaped junctions defining a plurality of laterally spaced vertical channel of length L_{VC} in said mesas with a uniform channel opening dimension of d_0 along the vertical channel;

(g) said top surface having ohmic contact forming the source of said transistor;

(h) said U-shaped junctions having ohmic contacts to the bottom of said U-shaped junctions forming the gate of said transistor;

(i) said semiconductor structure having ohmic contact on said bottom surface of said structure forming the drain of said transistor;

(j) said semiconductor structure having a top source layer more heavily doped than the doping densities of both sides of the vertical part of said U-shaped junctions;

2. A vertical junction field-effect power transistor according to claim **1** wherein

(a) said angle β is 90^0;

(b) said angle β is within the range of $90^0 \pm 5^0$;

(c) said angle β is within the range of $90^0 \pm 10^0$;

(d) said angle β is within the range of $90^0 \pm 20^0$;

(e) said angle β is within the range of $90^0 \pm 30^0$;

(f) said channel opening dimension d_0 is constant along and within said vertical channel;

(g) said channel opening dimension d_0 is within the range of $d_0 \pm 5\%d_0$ along and within said vertical channel;

(h) said channel opening dimension d_0 is within the range of $d_0 \pm 10\%d_0$ along and within said vertical channel;

(i) said channel opening dimension d_0 is within the range of $d_0 \pm 20\%d_0$ along and within said vertical channel;

(j) said channel opening dimension d_0 is within the range of $d_0 \pm 30\%d_0$ along and within said vertical channel;

(k) said channel length L_{VC} is in the range of 0.5 to 1.5um;

(l) said channel length L_{VC} is in the range of 1.5 to 2.5um;

(m) said channel length L_{VC} is in the range of 2.5 to 3.5um;

(n) said top source layer thickness is within the range of 0.2 to 2um;

(o) said top source layer thickness is within the range of 0.2 to 4um.

3. A vertical junction field-effect power transistor according to claim **2** wherein said plurality semiconductor layers including a first layer of first conductivity type for drain ohmic contact, a second layer of first conductivity type on top of said first layer as blocking and channel layer, a third layer of first conductivity type as top source layer.
4. A vertical junction field-effect power transistor according to claim **2** wherein said plurality semiconductor layers including a first layer of first conductivity type for drain ohmic contact, a second layer of first conductivity type on top of said first layer as blocking layer, a third layer of first conductivity type on top of said second layer as channel layer, and a fourth layer of first conductivity type on top of said third layer as top source layer.
5. A vertical junction field-effect power transistor according to claim **2** wherein said plurality semiconductor layers including a first layer of first conductivity type for drain ohmic contact, a second layer of first conductivity type on top of said first layer as buffer layer, a third layer of first conductivity type on top of said second layer as blocking and channel layer, a fourth layer of first conductivity type on top of said third layer as top source layer.
6. A vertical junction field-effect power transistor according to claim **2** wherein said plurality semiconductor layers including a first layer of first conductivity type for

drain ohmic contact, a second layer of first conductivity type on top of said first layer as buffer layer, a third layer of first conductivity type on top of said second layer as blocking layer, a fourth layer of first conductivity type on top of said third layer as channel layer, and a fifth layer of first conductivity type on top of said fourth layer as top source layer.

7. A bipolar vertical junction field-effect power transistor according to claim **2** wherein said bottom drain layer having conductivity type opposite to the conductivity type of said blocking and channel layer and said top source layer.

8. A vertical junction field-effect transistor according to claim **7** wherein said plurality semiconductor layers including a first layer of second conductivity type for drain ohmic contact, a second layer of first conductivity type on top of said first layer as blocking and channel layer, a third layer of first conductivity type on top of said second layer as top source layer.

9. A vertical junction field-effect power transistor according to claim **7** wherein said plurality semiconductor layers including a first layer of second conductivity type for drain ohmic contact, a second layer of first conductivity type on top of said first layer as blocking layer, a third layer of first conductivity type on top of said second layer as channel layer, and a fourth layer of first conductivity type on top of said third layer as top source layer.

10. A vertical junction field-effect power transistor according to claim **7** wherein said plurality semiconductor layers including a first layer of second conductivity type for drain ohmic contact, a second layer of second conductivity type on top of said first layer as buffer layer, a third layer of first conductivity type on top of said

second layer as blocking and channel layer, a fourth layer of first conductivity type on top of said third layer as top source layer.

11. A vertical junction field-effect power transistor according to claim **7** wherein said plurality semiconductor layers including a first layer of second conductivity type for drain ohmic contact, a second layer of second conductivity type on top of said first layer as buffer layer, a third layer of first conductivity type on top of said second layer as blocking layer, a fourth layer of first conductivity type on top of said third layer as channel layer, and a fifth layer of first conductivity type on top of said fourth layer as top source layer.